

REMARKS

Claims 1-6 and 8-28 were examined, with claims 1-6, 8, 10-21, and 23-28 rejected, and claims 9 and 22 have been indicated as containing allowable subject matter.

Turning to the prior art rejection, claims 1-6, 8, 10-21, and 23-28 have been rejected under 35 USC 103(a) as being unpatentable over Buxton et al. (U.S. Patent No. 5,925,133) in view of Bertin et al. (U.S. Patent No. 6,345,362). Applicant respectfully traverses this rejection for the reasons set forth below.

As the Examiner correctly states:

Buxton et al. does not teach controlling the power of the system by determining the energy available to the controller as well as controlling the peripheral devices depending on the energy available to the controller and the processor task being processed. In particular, Buxton et al. teaches a controller to process a task and a plurality of peripheral devices that are controlled to process the associated tasks. Buxton et al. does not teach that the energy of the peripheral devices is controlled by the processor task and the energy available to the controller.

Office Action, paragraph bridging pages 2 and 3.

Further, the Examiner's assessment resulting in the lack of inventiveness objection becomes incorrect at the portion within the Office Action stating:

Bertin et al. teaches ... an energy determination means for determining energy available to the controller (Col. 9 lines 56-59 Execution Unit); and a control means for controlling the controller depending on the energy available to the controller (Col. 9, lines 60-67), wherein the, control means is disposed due to the control of the plurality of peripheral devices in dependency on the processor task, the associated tasks and the energy available to the controller (Col. 9, lines 44-67).

In particular, the Examiner focuses on column 9, lines 56-64, of the disclosure of Bertin et al. The wording of this claim language is repeated in column 3, lines 3-18 of this disclosure with its meaning becoming clear from the context in which this wording is used. To be more precise, Berlin

et al. seeks "to control the power consumption of various functional units so as to present functional units in a high power state when instructions requiring their operation are to be executed and concomitantly to ensure power is not wasted on functional units, which are not involved in current instructions." (See column 2, lines 28-33.) Thus, Bertin et al. suggests powering-up or running at increased power levels units when an instruction is identified, which is about to be executed and requires the function (see column 2, lines 38-41). However, in suggesting this procedure, Bertin et al. faces a problem in that a "delay is occasioned in a transition of the power status of a functional unit from one power level to another" (see column 2, lines 46 and 47). In order to accommodate for this delay, a decoder unit checks as to whether any "of the functional units required for execution of a particular instruction are not at a high power state," wherein this "information is used in determining whether high speed operation for said instruction can be enabled." (See column 2, line 64, to column 3, line 2). Thus, the execution unit is for checking as to whether individual ones of the functionals have the required power status or levels. In particular, Bertin et al. reads:

In the event that one or more of the functional units do not have the required power status for execution at current processor speed, then the execution unit comes into play. A first option for the execution unit is to stall (or delay) the instruction stream for a time sufficient for a change in the Vt level of the particular functional unit ... wherein the alternative to stalling the instruction stream is to maintain the instruction stream, but to slow the process clock.

Column 3, lines 7-18.

Thus, to summarize, the portions of Bertin et al. as referred to by the Examiner with respect to the differential features not disclosed in Buxton merely relate to the execution unit of the Bertin et al. disclosure checking as to whether all the required functional units involved in a current instruction to be executed have already been provided with sufficient power.

Thus the claims are patentable over the applied references for at least these reasons.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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